UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,391	08/27/2003	Heather N. Bean	10018582-1	5319

22879 7590 08/23/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
KHAN, USMAN A	
ART UNIT	**PAPER NUMBER**
2622	
MAIL DATE	**DELIVERY MODE**
08/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,391	BEAN ET AL.	
	Examiner	Art Unit	
	Usman Khan	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments filed 5/18/2007, with respect to the rejection(s) of claim(s) 1 - 25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made. Since this is a new grounds of rejection, which was not done because of an amendment, this action is non-final.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 – 4, 7 – 8, 14, 16 – 17, 20 - 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Parulski et al. (US patent No. 5,668,597).

Regarding **claim 1,** Parulski et al. discloses a pixel-differentiated CCD imager architecture (figures 3, 10 and 11) comprising: a plurality of photo-sensing pixels arranged in a matrix (figures 3, 10 and 11), each pixel being classified according to type

from among a plurality of photo-sensing pixel types (figures 10 and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped; second, figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels); and read circuitry controllable to respectively read one or more of a second type of pixel independently of reading a first type of pixel (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq*. and column 6 lines 56 *et seq.*), the reading of one or more first type pixels representing a sampling of fewer than all of the plurality of pixels, the sampling being obtainable without having to read all of the plurality of pixels (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq*. and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped).

Regarding **claim 3**, as mentioned above in the discussion of claim 1, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that there are fewer second type pixels than first type pixels (figure 11 fewer active pixels then inactive pixels).

Regarding **claim 4**, as mentioned above in the discussion of claim 3, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that the second type pixels are arranged amongst the first type pixels such that the

second type pixels are uniformly distributed amongst the first type pixels (figures 10 and 11).

Regarding **claim 7**, as mentioned above in the discussion of claim 1, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that the first type pixels are organized into blocks; and the read circuitry is further controllable to read selected ones of blocks (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 8**, as mentioned above in the discussion of claim 7, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that the reading of the selected blocks of first type pixels represents a sampling of fewer than all of blocks without having to read all of the blocks (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 14,** Parulski et al. discloses a method of operating a CCD imager (figures 3, 10 and 11), the imager having a pixel-differentiated architecture that includes a plurality of photo-sensing pixels arranged in a matrix (figures 3, 10 and 11), each pixel being classified according to type from among a plurality of photo-sensing pixel-types including a first type and a second type of photo-sensing pixel (figures 10

and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped; second, figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels), the method comprising: reading one or more of the second type pixels independently of reading the first type pixels (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*), the reading of one or more second type pixels representing a sampling of fewer than all of the plurality of pixels, the sampling being obtainable without having to read all of the plurality of pixels (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped).

Regarding **claim 16**, as mentioned above in the discussion of claim 14, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches organizing the first type pixels into blocks; and selectively transferring information from selected ones of the blocks (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 17**, as mentioned above in the discussion of claim 16, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches selectively transferring fewer than all blocks without having to transfer

information from all of the blocks (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 20,** Parulski et al. discloses a pixel-differentiated CCD architecture (figures 3, 10 and 11) comprising: a first plurality of non-sampling arrays that include a first type of photosensor (figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped); and a second plurality of sampling arrays that include the first type of photosensor and a second type of photosensor, each sampling array being arranged so that sample-information from the second type photosensor can be transferred out of the sampling array without the sample-information having to be conveyed via any of the first type photosensors in the sampling array (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels along with the rest of pixels); and transfer means for transferring information out of one or more selected second type photosensors without also having to transfer information contained in first type photosensors (column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 21**, as mentioned above in the discussion of claim 20, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches the pixel-differentiated imager architecture comprising: a first plurality of blocks, each block having a second plurality of photo-sensing pixels arranged in a matrix (figure

10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels), each pixel being classified according to type from among a plurality of types including a first type and a second type of photo-sensing pixel (first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped; second, figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels); and read circuitry controllable to respectively read one or more of the second type pixels independently of reading the first type pixels, the read-circuitry not being controllable to read all of the pixels individually (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 22**, as mentioned above in the discussion of claim 21, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that the imager is implemented as a CCD (figures 3, 10 and 11 also column 4 lines 66 *et seq.*).

Regarding **claim 23**, as mentioned above in the discussion of claim 21, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that the read circuitry is controllable to read respectively read one or more of the blocks without having to read all of the blocks, the read-circuitry not being controllable to read all of the first type pixels in a block individually (figure 10 lines 1 – 2,

5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*).

Regarding **claim 24,** Parulski et al. discloses a digital camera (figure 1) comprising: a pixel-differentiated CCD imager architecture (figures 3, 10 and 11) including a plurality of photo-sensing pixels arranged in a matrix (figures 3, 10 and 11), each pixel being classified according to type from among a plurality of photo-sensing pixel-types including a first type and a second type of photo-sensing pixel (figures 10 and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped; second, figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels), and read circuitry controllable to respectively read one or more of the second type pixels independently of reading the first type pixels, the reading of one or more second type pixels representing a sampling of fewer than all of the plurality of pixels (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*), the sampling being obtainable without having to read all of the plurality of pixels (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped); and image processing means for controlling the read circuitry and processing the output of the pixel-differentiated CCD imager into a digital

representation of an image captured by the pixel-differentiated CCD imager (figures 1, 2A-2B reading out of images).

Regarding **claim 25,** Parulski et al. discloses a digital camera (figure 1) comprising: a pixel-differentiated CCD imager (figures 3, 10 and 11) including a first plurality of blocks (figures 10 and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped), each block having a second plurality of photo-sensing pixels arranged in a matrix (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read), each pixel being classified according to type from among a plurality of photo-sensing pixel-types including a first type and a second type of photo-sensing pixel (figures 10 and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped; second, figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels); and read circuitry controllable to respectively read one or more of the second type pixels independently of reading the first type pixels, the read-circuitry not being controllable to read all of the pixels individually (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*); and image processing means for controlling the read circuitry and processing the output of the pixel-differentiated CCD imager into a digital representation of an image captured by the pixel-differentiated CCD imager (figures 1, 2A-2B reading out of images).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (US patent No. 5,668,597) in further view of Examiners Official Notice.

Regarding **claims 2 and 15**, as mentioned above in the discussion of claims 1 and 14 respectively, Parulski et al. teaches all of the limitations of the parent claim. However, Parulski et al. fails to teach that operation of the read circuitry further including bucket brigading of charge.

The examiner takes Official Notice that it is old and well known in the art to use an operation of the read circuitry further including bucket brigading of charge in CCD sensors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate an operation of the read circuitry further including bucket brigading of charge as doing this would render a simpler low cost and more flexible device.

Claims 5 - 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (US patent No. 5,668,597) in further view of Sanpei (US PgPub 2001/0050715).

Regarding **claim 5**, as mentioned above in the discussion of claim 1, Parulski et al. teaches all of the limitations of the parent claim.

However, Parulski et al. fails to disclose a total area covered by the plurality of pixels is organized into a central portion and peripheral portion; the second type pixels are arranged amongst the first type pixels such that a density of second type pixels in the central portion is higher than in the peripheral portion. Sanpei, on the other hand teaches a total area covered by the plurality of pixels is organized into a central portion and peripheral portion; the second type pixels are arranged amongst the first type pixels such that a density of second type pixels in the central portion is higher than in the peripheral portion.

More specifically, Sanpei teaches a total area covered by the plurality of pixels is organized into a central portion and peripheral portion; the second type pixels are arranged amongst the first type pixels such that a density of second type pixels in the central portion is higher than in the peripheral portion.

One of ordinary skill in the art at the time the invention was made would have found it obvious to incorporate the teachings of Sanpei with the teachings of Parulski et al. because in paragraph 0012 Sanpei teaches that the present invention provides an image photographing apparatus and method in which the time required for adjustment such as automatic focus control, automatic photographic sensitivity control, or automatic

white balance control is reduced so that more accurate adjustment and more realistically photographed images may be achieved.

Regarding **claim 6**, as mentioned above in the discussion of claim 5, Parulski et al. in further view of Sanpei teaches all of the limitations of the parent claim. Additionally, Sanpei teaches that a distribution of the second type pixels amongst the first type pixels is, for each of the respective central and peripheral portions a uniform distribution (figure 4).

One of ordinary skill in the art at the time the invention was made would have found it obvious to incorporate the teachings of Sanpei with the teachings of Parulski et al. because in paragraph 0012 Sanpei teaches that the present invention provides an image photographing apparatus and method in which the time required for adjustment such as automatic focus control, automatic photographic sensitivity control, or automatic white balance control is reduced so that more accurate adjustment and more realistically photographed images may be achieved.

Claims 9 - 12, and 18 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (US patent No. 5,668,597) in further view of Yoshida (US patent No. 6,930,716).

Regarding **claim 9,** as mentioned above in the discussion of claim 1, Parulski et al. teaches all of the limitations of the parent claim. However, Parulski et al. fail to disclose the CCD imager architecture, wherein: the plurality is a first plurality; rows of

the matrix are grouped into a second plurality of banks, each bank being organized into a third plurality of arrays of the pixels; the pixel arrays are arranged to transfer information along a first direction; and the CCD imager architecture further comprises a fourth plurality of information-transfer linear arrays of information-transferring cells, each information-transfer array being associated with at least one bank and arranged adjacent to a side of the at least one bank such that two neighboring banks are separated by an information-transferring linear-array. Yoshida, on the other hand discloses that the CCD imager architecture, wherein: the plurality is a first plurality; rows of the matrix are grouped into a second plurality of banks, each bank being organized into a third plurality of arrays of the pixels; the pixel arrays are arranged to transfer information along a first direction; and the CCD imager architecture further comprises a fourth plurality of information-transfer linear arrays of information-transferring cells, each information-transfer array being associated with at least one bank and arranged adjacent to a side of the at least one bank such that two neighboring banks are separated by an information-transferring linear-array.

More specifically, Yoshida teaches that each the CCD imager architecture, wherein: the plurality is a first plurality (figure 2); rows of the matrix are grouped into a second plurality of banks (figure 2), each bank being organized into a third plurality of arrays of the pixels (figure 2); the pixel arrays are arranged to transfer information along a first direction; and the CCD imager architecture further comprises a fourth plurality of information-transfer linear arrays of information-transferring cells (figure 2), each information-transfer array being associated with at least one bank and arranged

adjacent to a side of the at least one bank such that two neighboring banks are separated by an information-transferring linear-array (figure 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yoshida with the teachings of Parulski et al. because in column 1 lines 16 et seq. Yoshida teaches that the image pickup structure taught in the invention will increase sensitivity of the device this would render better image quality.

Regarding **claim 10,** as mentioned above in the discussion of claim 9, Parulski et al. in further view of Yoshida teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that the CCD imager wherein: each pixel array includes pixels of a first type (figures 10 and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped); a predetermined number of the pixel arrays are sampling arrays that further include a second type of pixel (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*); each sampling array is arranged so that sample-information from the second type pixel can be transferred to the associated information-transfer array without the sample-information having to be conveyed via any of the first type pixels in the sampling array (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels

being dumped); the sampling array being controllable to read the second type pixel without having to read all of the first type pixels in the sampling array (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped).

Regarding **claim 11,** as mentioned above in the discussion of claim 10, Parulski et al. in further view of Yoshida teaches all of the limitations of the parent claim. Additionally, Yoshida teaches that each pixel array is configured as a linear array of pixels that is controllable to transfer information in a second direction perpendicular to the first direction (figure 2).

Regarding **claim 12,** as mentioned above in the discussion of claim 11, Parulski et al. in further view of Yoshida teaches all of the limitations of the parent claim. Additionally, Yoshida teaches that each linear array is arranged into a space-filling configuration that covers an area that would otherwise correspond to a two-dimensional array (figure 2).

Regarding **claim 18,** as mentioned above in the discussion of claim 14, Parulski et al. teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that each pixel array includes first type pixels (figures 10 and 11; first, figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being

dumped), and a predetermined number of the pixel arrays are sampling arrays that further include a second type pixel figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*); and the method further comprises transferring sample-information from the second type pixel to the associated information-transfer array (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped) without having to convey the sample-information via any of the first type pixels in the sampling array (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped).

However, Parulski et al. fail to disclose that the plurality is a first plurality; rows of the matrix are grouped into a second plurality of banks, each bank being organized into a third plurality of arrays of the pixels; and the pixel-differentiated architecture further includes a fourth plurality of information-transfer linear arrays of information-transferring cells, each information-transfer array being associated with at least one bank and arranged adjacent to a side of the at least one bank such that two neighboring banks are separated by an information-transferring linear-array. Yoshida, on the other hand discloses that the plurality is a first plurality (figure 2); rows of the matrix are grouped into a second plurality of banks, each bank being organized into a third plurality of

arrays of the pixels (figure 2); and the pixel-differentiated architecture further includes a fourth plurality of information-transfer linear arrays of information-transferring cells (figure 2), each information-transfer array being associated with at least one bank and arranged adjacent to a side of the at least one bank such that two neighboring banks are separated by an information-transferring linear-array (figure 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yoshida with the teachings of Parulski et al. because in column 1 lines 16 et seq. Yoshida teaches that the image pickup structure taught in the invention will increase sensitivity of the device this would render better image quality.

Regarding **claim 19,** as mentioned above in the discussion of claim 18, Parulski et al. in further view of Yoshida teaches all of the limitations of the parent claim. Additionally, Parulski et al. teaches that reading of the second type pixel of a sampling array without having to read all of the first type pixels in the sampling array (figure 10 lines 1 – 2, 5 – 6, and 9 – 10 also figure 11 lines 1 – 2 and 9 - 10; active pixels being read; column 2 lines 66 *et seq.* and column 6 lines 56 *et seq.*; also figure 10 lines 3 - 4, 7 - 8, and 11 - n also figure 11 lines 3 - 8 and 11 - 16; inactive pixels being dumped).

Claims 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (US patent No. 5,668,597) in further view of Yoshida (US patent No. 6,930,716) in further view of Yamamoto (US patent No. 6,549,644).

Regarding **claim 13,** as mentioned above in the discussion of claim 12, Parulski et al. in further view of Yoshida teaches all of the limitations of the parent claim. However, Parulski et al. in further view of Yoshida fail to teach that the space-filling configuration is one of a raster and a piece-wise continuous spiral. Yamamoto, on the other hand discloses that the space-filling configuration is one of a raster and a piece-wise continuous spiral.

More specifically, Yamamoto teaches that the space-filling configuration is one of a raster and a piece-wise continuous spiral (figure 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamamoto with the teachings of Parulski et al. in further view of Yoshida because in column 1 lines 66 et seq. Yamamoto teaches that doing so will result will raise the processing speed which will result in a faster system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Usman Khan whose telephone number is (571) 270-1131. The examiner can normally be reached on Mon-Thru 6:45-4:15; Fri 6:45-3:15 or Alt. Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Usman Khan
08/17/2007
Patent Examiner
Art Unit 2622

LIN YE
SUPERVISORY PATENT EXAMINER